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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,422	11/21/2003	Paul Rudeck	400.178US02	3392

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,422	RUDECK, PAUL	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0904
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong, U.S. Patent 5,414,287.

Hong shows the invention as claimed including a method for fabricating non-volatile memory cells, the method comprising: forming a pillar of silicon 36 vertically extending above a substrate 30; implanting a drain region 42 in a top of the pillar; implanting first and second source regions 40 in the substrate and adjacent to the pillar; wherein the first and second source regions are located on opposite sides of the pillar; forming floating gates 48 adjacent to and on opposite sides of the pillar; forming first and second control gates 54 insulated from the floating gates and located on opposite sides of the pillar; and forming a wordline parallel to and between the first and second control gates (note that both the control gate and wordline are represented by reference number 54 so the control gate can be represented by the regions of layer 54 overlying the respective floating gates and the wordline can be represented by the portion of layer 54 between these regions—for a description of the process, see figs. 3-8 and col. 4-line 7 to col. 5-line 44).

Regarding claim 2, note that the floating gates 48 and control gates 54 are formed of polysilicon.

With respect to claim 4, note that forming the pillar of silicon comprises etching the substrate to form first and second perpendicular grooves (see fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, U.S. Patent 5,414,287 in view of Kawata, U.S. Patent 6,157,061.

Hong is applied as above but fails to expressly disclose wherein the control gates are fabricated using polysilicon and silicide.

Kawata discloses forming control gates 106a,106b using polysilicon and silicide (see col. 3-lines 45-51). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hong so as to form the control gates of polysilicon and silicide as suggested by Kawata because this is shown to be a suitable material for a control gate electrode and is well known to provide a higher conductivity than a polysilicon electrode.

Claims 5-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, U.S. Patent 5,414,287 in view of Noble et al., U.S. Patent 6,486,027.

Hong is applied as above but fails to expressly disclose wherein the first groove is filled with an insulating material prior to etching the second groove, forming a set of trenches perpendicular to the device trenches which are filled with oxide, depositing a layer of nitride prior to etching the trenches, and depositing a layer of oxide prior to depositing the nitride.

Noble et al. discloses a memory architecture in which first grooves 605 are formed filled with oxide prior to forming the second device grooves, wherein a nitride layer 610 and oxide layer 520 is formed prior to etching the grooves (see figs. 8-16 and col. 12-line 16 to col. 14-line 43). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the

process of Hong so as to include the architecture using the process of Noble et al. because such an architecture allows for a high integration memory cell.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, U.S. Patent 5,414,287 in view of Noble et al., U.S. Patent 6,486,027 as applied to claims 5-8 and 11-12 above, and further in view of Kawata, U.S. Patent 6,157,061.

Hong is applied as above but fails to expressly disclose wherein the control gates are fabricated using polysilicon and silicide.

Kawata discloses forming control gates 106a,106b using polysilicon and silicide (see col. 3-lines 45-51). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hong modified by Noble et al. so as to form the control gates of polysilicon and silicide as suggested by Kawata because this is shown to be a suitable material for a control gate electrode and is well known to provide a higher conductivity than a polysilicon electrode.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, U.S. Patent 5,414,287 in view of Noble et al., U.S. Patent 6,486,027 as applied to claims 5-8 and 11-12 above, and further in view of Mori, U.S. Patent 5,071,782.

Hong and Noble et al. are applied as above but fail to expressly disclose fabricating an electrically conductive vertically stacked source/drain line structure. Mori discloses forming a vertically stacked source/drain line structure (see col. 5-line 58 to

col. 6-line 40). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hong modified by Noble et al. so as to form a vertically stacked source/drain structure because this will increase the access time of the memory device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

September 29, 2004